ABSTRACT OF THE DISCLOSURE

A ferroelectric memory device includes a memory cell array and a peripheral circuit section. The memory cell array, in which memory cells are arranged in a matrix, includes first signal electrodes, second signal electrodes which are arranged in a direction so as to intersect the first signal electrodes, and a ferroelectric layer disposed at least at intersection regions between the first signal electrodes and the second signal electrodes. The peripheral circuit section includes circuits for selectively allowing information to be written into or read from the memory cells, such as a first driver circuit, a second driver circuit, and a signal detection circuit. The memory cell array and the peripheral circuit section are disposed in different layers so as to be layered. This ferroelectric memory device can significantly increase the degree of integration of the memory cells and decrease the chip area.